



AF/2811  
IFW  
\$

PTO/SB/21 (05-03)

Approved for use through 04/30/2003. OMB 0651-0031

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

<b>TRANSMITTAL FORM</b>  (to be used for all correspondence after initial filing)	Application Number	09/915,145
	Filing Date	July 25, 2001
	First Named Inventor	Takeshi Nogami
	Art Unit	2811
	Examiner Name	Thomas J. Magee
Total Number of Pages in This Submission	Attorney Docket Number	075834.00096

ENCLOSURES (Check all that apply)		
<input checked="" type="checkbox"/> Fee Transmittal Form	<input type="checkbox"/> Drawing(s)	<input type="checkbox"/> After Allowance communication to Group
<input checked="" type="checkbox"/> Fee Attached	<input type="checkbox"/> Licensing-related Papers	<input checked="" type="checkbox"/> Appeal Communication to Board of Appeals and Interferences
<input type="checkbox"/> Amendment/Reply	<input type="checkbox"/> Petition	<input type="checkbox"/> Appeal Communication to Group (Appeal Notice, Brief, Reply Brief)
<input type="checkbox"/> After Final	<input type="checkbox"/> Petition to Convert to a Provisional Application	<input type="checkbox"/> Proprietary Information
<input type="checkbox"/> Affidavits/declaration(s)	<input type="checkbox"/> Power of Attorney, Revocation	<input type="checkbox"/> Status Letter
<input type="checkbox"/> Extension of Time Request	<input type="checkbox"/> Change of Correspondence Address	<input checked="" type="checkbox"/> Other Enclosure(s) (please identify below):
<input type="checkbox"/> Express Abandonment Request	<input type="checkbox"/> Terminal Disclaimer	Post Card
<input type="checkbox"/> Information Disclosure Statement	<input type="checkbox"/> Request for Refund	
<input type="checkbox"/> Certified Copy of Priority Document(s)	<input type="checkbox"/> CD, Number of CD(s) _____	
<input type="checkbox"/> Response to Missing Parts/Incomplete Application	Remarks	
<input type="checkbox"/> Response to Missing Parts under 37 CFR 1.52 or 1.53	The Commissioner is hereby authorized to charge any fees due or to credit any overpayment to Deposit Account No. 50-1794.	

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT	
Firm or Individual name	Robert J. Depke, Holland & Knight LLP 131 South Dearborn Street, 30th Floor, Chicago, IL 60603
Signature	
Date	10/22/04

CERTIFICATE OF TRANSMISSION/MAILING	
I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below.	
Typed or printed name	Robert J. Depke (Reg. No. 37,6)
Signature	
Date	10/22/04

This collection of information is required by 37 CFR 1.5. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

**Appl. No.:** 09/915,145 **Confirmation No.:** 6448  
**Applicant:** Takeshi Nogami  
**Filed:** July 25, 2001  
**TC/A.U.:** 2811  
**Examiner:** Thomas J. Magee  
**Docket No.:** 075834.00096  
**Customer No.:** 33448

**APPEAL BRIEF**

**I. REAL PARTY IN INTEREST**

The real party in interest is Sony Corporation as a result of transfer of all right, title and interest to the subject matter of this Application Serial No. 09/915,145, via the Assignment recorded in the Patent Office in Reel 012-516 Frame 0057 on January 18, 2002.

**II. RELATED APPEALS AND INTERFERENCES**

Applicants and the undersigned are currently unaware of any related appeals or interferences in relation to the instant Appeal.

**III. STATUS OF CLAIMS**

The claims currently stand in condition as modified by Amendment A dated October 3, 2002 amending claims 1-6 and adding new claims 8-11, which has been entered by the Examiner, as well as Amendment B dated June 10, 2003 amending claims 1, 5, and 8,

canceling claim 10, and adding new claims 12 and 13, as well as Amendment C dated October 14, 2003 amending claims 12 and 13, which has been entered by the Examiner. Accordingly, claims 1-9 and 10-13 are currently pending, and stand in condition as set forth in the attached Appendix of Claims on Appeal.

#### **IV. STATUS OF AMENDMENTS**

All of the amendments noted above in the status of the claims have been entered and no amendment has been submitted subsequent to the amendment dated October 14, 2003 which has been entered by the Examiner. Accordingly, the claims stand as set forth in the attached Appendix.

#### **V. SUMMARY OF INVENTION**

Applicant's invention relates to the field of copper wirings for semiconductor devices. More specifically, the instant invention is directed to an improvement in the structure and method of manufacturing copper wirings for semiconductor devices such that a practical oxidation resistant copper wiring is provided and furthermore, silicon dioxide, a traditional and inexpensive semiconductor material which has been avoided thus far in copper wiring semiconductors, can be easily used.

For example, the specification notes that copper wirings are easily oxidized even at low temperatures see page 1 in the last line through page 2 at lines 1-5. One traditional approach to overcoming this problem is the use of an anti-oxidation film such as silicon nitride or silicon carbide but the dielectric constants are undesirable for high speed wirings. See page 2 at lines 6-14. The specification also notes that CoWP has previously been

proposed in order to prevent oxidation of the copper wirings but CoWP alone is undesirably eroded during the removal of copper in the formation of the wirings via fluorinated acid.

In order to overcome the deficiencies and problems of the prior art, the inventors have discovered that CoWP can be used with improved results by providing a cobalt silicide as a clad layer over CoWP layer. Advantageously, the cobalt silicide clad layer has resistance to oxidation and the cobalt silicide layer also is resistant to fluorinated acid. See specifically Applicants' Summary of the Invention at page 3, lines 11-16. The resultant structure prevents diffusion of copper and is also both oxidation resistant and resistant to removal via fluorinated acid. See page 3 at lines 19-22. Independent claims 1 and 8 specify the underlying structure described above with an additional oxygen including layer or silicon dioxide layer that is described below.

In accordance with another aspect of the invention, the manufacturing process of the instant invention reduces the number of steps needed to manufacture a copper-wiring based semiconductor, thereby lowering the complexity and costs of a copper wiring manufacturing process involving said oxide insulators. Specifically, in accordance with a preferred embodiment of the invention, a CoWP layer formed over a copper wiring is exposed in a silane gas system in order to easily provide a cobalt silicide cladding layer. See page 3 at lines 23-30. The cobalt silicide thus protects the CoWP layer and prevents oxidation and corrosion by fluorinated acid. As described in more detail below, in accordance with another aspect of the instant invention, a silicon dioxide film can thereafter be easily formed.

In accordance with the instant invention, as shown in Figure 1, a wiring groove 12 formed in an insulation 11 has a barrier layer 13 formed therein. See page 4 lines 25-32. A copper wiring 14 is formed over the barrier layer 13 and a CoWP layer 15 is provided on the copper wiring 14. Thereafter, a clad layer preferably comprised of a cobalt silicide layer 16 is formed on the CoWP layer 15. See Applicants' specification at page 5 in lines 8-24 and Figure 1. The structure illustrated in Figure 1 is also described in claims 1, 8 and 15 except for the oxygen including layer also set forth in these claims. The description of the oxygen including layer is described below with reference to the method of manufacture disclosed in the specification.

For example, claim 1 specifies a conductive member which is the described copper wiring 14 and a cobalt including layer which is the referenced CoWP layer 15. The clad layer specified in claim 1 is the cobalt silicide 16.

The method of manufacture set forth in independent claim 5 is described in the Applicants' specification beginning on page 6 with reference to Figures 2A and 2B. Lines 5-26 of page 6 describe the formation of the copper wiring 14 in the groove 12 of the insulation 11 with the barrier layer 13 as a separation. Thereafter, lines 27-31 describe formation of the CoWP layer 15. Subsequently, this structure is exposed in a silane reaction gas which reacts with the CoWP in order to form the cobalt silicide clad layer 16 as illustrated in Figure 2B. See page 6 in the last 2 lines through page 7 at lines 1-7.

Advantageously, as noted in lines 8-24, the oxidation and undesired etching of the CoWP layer via fluorinated acid are overcome by the convenient formation of the clad layer formed of cobalt silicide.

Another feature of the instant invention is that a silicon dioxide insulating layer can be conveniently formed over the cobalt silicide clad layer as described in page 8 at lines 7-19. More specifically, as described at lines 15-19, formation of a silicon dioxide insulating film can be made easily in the same processing chamber after formation of the cobalt silicide clad layer 16 without the need for a new apparatus. This is the oxygen including layer referenced in the last line of claim 1 and is also found in claim 6 as well as the last limitation of claim 8 and 12.

As detailed below, the prior art of record fails to either teach or suggest the subject matter claimed in the instant application as summarized herein.

## **VI ISSUES PRESENTED FOR REVIEW**

Based on the Examiner's rejections set forth in the Final office action dated November 18, 2003, the issues presented on appeal are as follows:

- I. Whether the *Lopatin* (United States Patent No. 6,259,160), *Dubin* (United States Patent No. 5,695,810), *Shacham-Diamand* "High Aspect Ratio Quarter-Micron Electroless Copper Integrated Technology," *Wilson* "Handbook of Multilevel Metallization for Integrated Circuits," and *Pasch* (United States Patent No. 5,689,134) references provide the requisite teaching or suggestion to combine the disparate technologies contained in each reference in order to render obvious the subject matter of claims 1 – 4 as stated in paragraph 2 of the Final office action dated November 18, 2003.

- II. Whether the *Lopatin* (United States Patent No. 6,259,160), *Dubin* (United States Patent No. 5,695,810), *Shacham-Diamand* "High Aspect Ratio Quarter-Micron Electroless Copper Integrated Technology," and *Wilson* "Handbook of Multilevel Metallization for Integrated Circuits," references provide the requisite teaching or suggestion to combine the disparate technologies contained in each reference in order to render obvious the subject matter of claims 5, 7, and 11, as set forth in paragraph 4 of the Final office action dated November 18, 2003.
- III. Whether the *Lopatin* (United States Patent No. 6,259,160), *Dubin* (United States Patent No. 5,695,810), *Shacham-Diamand* "High Aspect Ratio Quarter-Micron Electroless Copper Integrated Technology," *Wilson* "Handbook of Multilevel Metallization for Integrated Circuits," and *Sherman* "Chemical Vapor Deposition for Microelectronics," references provide the requisite teaching or suggestion to combine the disparate technologies contained in each reference in order to render obvious the subject matter of claim 6 as asserted by the Examiner in paragraph 6 of the Final office action dated November 18, 2003.
- IV. Whether the *Lopatin* (United States Patent No. 6,259,160), *Dubin* (United States Patent No. 5,695,810), *Shacham-Diamand* "High Aspect Ratio Quarter-Micron Electroless Copper Integrated Technology," *Wilson* "Handbook of Multilevel Metallization for Integrated Circuits," *Sherman* "Chemical Vapor Deposition for Microelectronics," and *Pasch* (United States Patent No. 5,689,134) references

provide the requisite teaching and suggestion to combine the disparate technologies contained in each reference in order to render obvious the subject matter of claims 8, 9, 12 and 13 as asserted by the Examiner in paragraph 7 of the Final office action dated November 18, 2003.

V.

#### **VII GROUPING OF CLAIMS**

Based on the Examiner's rejections set forth in the Final office action dated November 18, 2003, the claims are grouped together as follows:

Claims 1 – 4, 8-9 and 11 stand together. Claims 5, 7 and 11 stand together. Claims 6, 12 and 13 stand together.

#### **VIII ARGUMENT**

Applicants respectfully submit that the prior art references of record, whether considered alone, or in combination, fail to either teach or suggest Applicant's presently claimed invention. Applicant notes that the references of record fail to provide any teaching or suggestion whatsoever regarding the specified semiconductor device and manufacturing method set forth in the above groups of claims. As detailed below, the rejections set forth by the Examiner are improper.

##### **A. The Cited References Fail to Teach or Suggest the Claimed Invention as specified in Claims 1 – 4.**

The references cited by the Examiner, whether considered alone or in combination, fail to provide the requisite teaching or suggestion for rendering the subject matter of claims



1 – 4 invalid as being either obvious or anticipated. The numerous references cited by the Examiner in support of the rejection of claims 1- 4 include: *Lopatin* (United States Patent No. 6,259,160), *Dubin* (United States Patent No. 5,695,810), *Shacham-Diamand* “High Aspect Ratio Quarter-Micron Electroless Copper Integrated Technology,” *Wilson* “Handbook of Multilevel Metallization for Integrated Circuits,” and *Pasch* (United States Patent No. 5,689,134).

In general, claims 1 – 4 specify a semiconductor device comprising a conductive member, a cobalt including layer formed over the conductive member, a clad layer formed over the cobalt including layer, and an oxygen-containing layer formed over the clad layer.

The current invention is directed to solving the problem in the industry of having to use more expensive insulating materials in semiconductors with copper interconnects because of the corrosive nature of the copper wiring in the presence of traditional oxide insulating compounds such as Silicon Dioxide (SiO<sub>2</sub>). Applicant’s invention provides for a device and method for fabricating a copper-based semiconductor such that low-cost oxide-based insulating layers can be utilized without damage to pre-existing copper interconnects by forming a cobalt silicide layer over a cobalt tungsten phosphor layer formed over the copper interconnect. Fundamentally, there is simply no teaching whatsoever in the cited art relating to either the cobalt silicide or cladding layer and the oxygen containing layer formed over the cobalt silicide.

The significant deficiency of *Lopatin* with respect to claims 1 – 4 is that there is simply no teaching or suggestion whatsoever regarding the use of oxide-based insulating layers or the formation of a cobalt silicide clad layer to protect the cobalt tungsten phosphor layer and the underlying copper interconnect from oxidation and fluorinated acid treatments.

*Lopatin* actually teaches away from using oxides with copper and CoWP semiconductor devices by disclosing alternative materials such as: “polyarylene ether (PAE), fluorinated aromatic ether (FLARE), fluorinated polyimide (FPI), benzocyclobutene (BCB), hydrogen silsequioxane (HSQ), methyl silsequioxane (MSQ), or xerogel and fluorinated glass.” (*Lopatin*, Column 4 lines 40 – 49). The Examiner recognizes this deficiency and relies on other references for the subject matter of the cobalt silicide cladding layer.

The remaining references however are similarly deficient. Specifically, the *Shacham-Diamond* reference, the Examiner’s primary reference teaches the creation of a Cu/CoWP/Co/Si structure by depositing *the CoWP barrier layer* followed by Cu which is thereafter annealed to form the resulting structure. Contrary to the Examiner’s assertions, neither this reference nor any other reference teaches or suggests that cobalt and silicon layers should be separately formed over a CoWP layer that is located on a copper wiring.

A careful reading of the reference confirms that the only statement related to cobalt and silicon layer is on page 14 wherein the reference states: “The RBS spectrum of the Cu/CoWP/Co/Si structure formed by electroless CoWP barrier / Cu deposition and annealed at 400 C for 60 min. in vacuum . . . . showed no interdiffusion in deposited films. The reference merely indicates that the specified structure containing the referenced layers is so formed. Neither this portion nor any remaining portion of the reference indicates that separate Co and silicon layers are formed on the CoWP layer and annealed as asserted by the Examiner. This assertion is only an unsupported conclusion of the Examiner as to the formation of the separate layers prior to annealing. This is the only reference cited for the teaching concerning the cobalt silicide cladding layer or any other cladding layer for that

matter that is formed over a CoWP layer on a copper wiring. For this reason alone the rejection is improper and should be withdrawn.

In addition, the *Shacham-Diamand* reference fails to disclose the use of oxide-based insulators formed over the cobalt-silicide layer, as specified by Applicants in claims 1-4. In fact, the *Shacham-Diamand* authors teach away from such a result, as the sole stated purpose of applying the cobalt-silicide layer is to reduce the resistance of the CoWP film, stating said decrease in resistance to be approximately  $5 \mu\Omega/\text{cm}$ . At no point do the authors disclose the use of an oxygen-containing layer applied over the cobalt silicide layer. While Examiner has stated that it was well-known in the art to use oxygen containing layers in metal-interconnect structures, neither the *Wilson* nor the *Pasch* reference cited by the Examiner teaches or suggests using an oxygen containing layer applied over a cobalt tungsten phosphor layer or over a cobalt silicide layer formed thereon.

*Dubin* teaches the use of copper interconnects and oxide-based insulators separated solely by a CoWP layer. However, such a device has disadvantages in that it lacks the additional protection provided by the cobalt silicide layer. The single CoWP layer fails to prevent fluorinated acid reduction and fails to prevent oxidation when a semiconductor is placed in an oxygen rich atmosphere for formation of an oxide-layer via a CVD process. This is especially true when attempting to further deposit silicon dioxide via exposure to an oxygen containing chemical vapor epitaxy atmosphere, which will oxidize the protective CoWP film and potentially the copper it is protecting.

Applicant's invention as specified in claim 1 requires a semiconductor device containing 1) a conductive member; 2) a cobalt containing layer formed over said conductive member; 3) a clad layer formed over said cobalt including layer, *and* 4) an oxygen-containing

layer formed over said clad layer. None of the references cited by the Examiner teach or suggest such a structure containing all four semiconductor layers. Further, most of the references actually *teach away* from the specified structure. While one may be motivated to, in hind sight, find such a combination to be obvious in light of its currently disclosed benefits, such a basis for rejection has been held to be inapplicable by the US Court of Appeals for the Federal Circuit.

The Federal Circuit has held that “Combining prior art references without evidence of such a suggestion, teaching, or motivation simply takes the inventor’s disclosure as a blueprint for piecing together the prior art to defeat patentability.” *In re Dembiczak*, 50 U.S.P.Q.2d 1614, 1617. (C.A.F.C. 1999). Further, “the best defense against the subtle but powerful attraction of a hindsight-based obviousness analysis is rigorous application of the requirement for a showing of the teaching or motivation to combine prior art references.” *In re Gartside*, 53 U.S.P.Q.2d 1769 (C.A.F.C. 2000), citing, *In re Dembiczak*, 50 USPQ2d at 1617.

Accordingly, in light of the foregoing the rejection of claims 1 – 4 is improper and should therefore be withdrawn.

**B. The Cited References Fail to Teach or Suggest the Claimed Invention as specified in Claims 5, 7, and 11.**

None of the references cited by the examiner, alone or in combination, provides the requisite teaching or suggestion for rendering the subject matter of claims 5, 7, and 11 invalid as being obvious or anticipated. These references include: *Lopatin* (United States Patent No. 6,259,160), *Dubin* (United States Patent No. 5,695,810), *Shacham-Diamand* “High Aspect

Ratio Quarter-Micron Electroless Copper Integrated Technology,” and *Wilson* “Handbook of Multilevel Metallization for Integrated Circuits.”

Claims 5, 7, and 11 specify a method for manufacturing a semiconductor device containing a conductive member comprising the steps of: forming a cobalt including layer on a conductive member, and subsequently forming a cobalt silicide layer in a single processing step by exposing said cobalt including layer to a silane gas atmosphere. The current invention is directed to solving the problem in the industry of having to use more expensive insulating materials in semiconductors with high-performance yet highly corrosive metal, such as copper, because of the reaction of the metal wiring in the presence of traditional oxide insulating compounds such as Silicon Dioxide (SiO<sub>2</sub>). Applicant’s invention provides for a method for fabricating such a high-performance copper conductor semiconductor device such that low-cost oxide-based insulating layers can be utilized without damage to the copper interconnects.

The significant deficiency of *Lopatin* with respect to claims 5, 7, and 11 is that there is simply no teaching or suggestion whatsoever regarding the formation of a cobalt silicide clad layer to protect the cobalt tungsten phosphor layer and the underlying copper interconnect from oxidation and fluorinated acid treatments during subsequent exposure to an oxygen-containing silane atmosphere. The Examiner recognizes this deficiency and relies on other references for the subject matter of the cobalt silicide cladding layer.

The remaining references however are similarly deficient. Specifically, the *Shacham-Diamond* reference, the Examiner’s primary reference teaches the creation of a Cu/CoWP/Co/Si structure by depositing *the CoWP barrier layer* followed by Cu which is thereafter annealed to form the resulting structure. Contrary to the Examiner’s assertions,

neither this reference nor any other reference teaches or suggests that cobalt and silicon layers should be separately formed over a CoWP layer that is located on a copper wiring.

A careful reading of the reference confirms that the only statement related to cobalt and silicon layer is on page 14 wherein the reference states: "The RBS spectrum of the Cu/CoWP/Co/Si structure formed by electroless CoWP barrier / Cu deposition and annealed at 400 C for 60 min. in vacuum . . . . showed no interdiffusion in deposited films. The reference merely indicates that the specified structure containing the referenced layers is so formed. Neither this portion nor any remaining portion of the reference indicates that separate Co and silicon layers are formed on the CoWP layer and annealed as asserted by the Examiner. This assertion is only an unsupported conclusion of the Examiner as to the formation of the separate layers prior to annealing. This is the only reference cited for the teaching concerning the cobalt silicide cladding layer or any other cladding layer for that matter that is formed over a CoWP layer on a copper wiring. For this reason alone the rejection is improper and should be withdrawn.

Furthermore, even if one were to make the conclusion asserted by the Examiner, the rejection is nevertheless improper. Applicant's invention specified in claims 5, 7 and 11 is directed to a process by which no separate deposition of cobalt or silicon layers is required. Rather, after deposition of the CoWP layer and within the same processing apparatus, the device (including the copper and CoWP layer depositions) is heated up in an atmosphere of silane gas, thereby forming a layer of CoSi over the CoWP layer without the need for separate deposition of cobalt and silicon layers, and without the need for separate apparatus to anneal the two layers.

The Examiner has asserted that Applicant's method of creating a CoSi layer in fewer steps than in the prior art is non-inventive in view of the holding in *In re Tatincloux*, 108 U.S.P.Q. 125 (CCPA 1955). However, the CCPA distinguished that case on its facts in *In re Freed*, 165 U.S.P.Q. 570 (C.C.P.A. 1970). In considering the *Tatincloux* case, the CCPA held that "As can be seen, however, the process steps involved were entirely physical in nature. What was said there regarding the obviousness 'of performing simultaneously operations which have previously been performed in sequence,' might have been correct for the facts of that case. We are not prepared, however, to draw from that opinion the broad proposition which the Patent Office has ascribed to it." *In re Freed*, 165 U.S.P.Q. at 570. The court went on to hold that the reduction in the number of steps involving chemical reactions was novel over the prior art because "it seems more logical and reasonable to infer that one teaching a chemical reaction process would set out the least number of reactions thought necessary to accomplish the desired objective. Thus, one skilled in the art who reads the teaching would have to presume that if the reactants were not combined in the manner shown, some adverse side reaction or no reaction at all would occur." *In re Freed*, 165 U.S.P.Q. at 570.

In this case, the physical and chemical methods disclosed in the prior art do not even provide the separate formation of cobalt and silicon on a CoWP layer as argued by the Examiner. Even if the Examiner's assertions were found to be true in some other reference the rejections would still be improper. Applicants, just as in the *Freed* case, are not simply doing "simultaneously" that which was previously done "in sequence." Rather, an entirely different process is used in which: 1) a CoWP layer is deposited on a copper wiring, and 2) simultaneously, the semiconductor device is heated and the CoWP is exposed to a silane

atmosphere and a cobalt silicide layer is formed over the CoWP layer as a result of the chemical reaction. This method saves two separate steps over the prior art by utilizing an *entirely* different method than that disclosed in the *Shacham-Diamand* reference, and allows for reduced equipment costs, reduced production costs, and reduced time-to-product.

The Examiner further cites the *Dubin* reference in rejecting the claims but Durbin teaches using copper interconnects and oxide-based insulators separated solely by a CoWP layer, and fails to teach or suggest any formation of a cobalt silicide layer. Such a device has disadvantages in that it lacks the additional protection provided for by the cobalt silicide layer. The single CoWP layer fails to prevent fluorinated acid reduction and fails to prevent oxidation of the CoWP layer and possibly the metal interconnect when the semiconductor device is subsequently placed in an oxygen rich atmosphere for formation of an oxide-layer via a CVD process.

Applicant's invention specified in claims 5, 7 and 11 is directed to a method of manufacturing a semiconductor device 1) containing a conductive member comprising the steps of: 2) forming a cobalt including layer over the conductive member, 3) forming a cobalt silicide layer on a surface of the cobalt including layer by use of a silane gas atmosphere. None of the references cited by the Examiner teach or suggest such a structure containing these three specific method steps. Further, most of the cited references actually teach away from it.

Accordingly, in light of the foregoing the rejection of claims 5, 7, and 11 is improper and should therefore be withdrawn.



**C. The Cited References Fail to Teach or Suggest the Claimed Invention as specified in Claims 6, 12, and 13.**

None of the references cited by the Examiner, alone or in combination, provides the requisite teaching or suggestion for rendering the subject matter of claims 6, 12, and 13 invalid as being obvious or anticipated. These references include: *Lopatin* (United States Patent No. 6,259,160), *Dubin* (United States Patent No. 5,695,810), *Shacham-Diamand* "High Aspect Ratio Quarter-Micron Electroless Copper Integrated Technology," and *Wilson* "Handbook of Multilevel Metallization for Integrated Circuits," *Sherman* "Chemical Vapor Deposition for Microelectronics,"

Claims 6, 12, and 13 specify a method for manufacturing a semiconductor device containing a conductive member comprising the steps of: forming a cobalt including layer over a conductive member, forming a cobalt silicide layer over said cobalt including layer by use of a silane gas atmosphere, and finally forming an oxygen-including layer over said cobalt silicide layer by adding oxygen to the silane gas atmosphere.

The current invention is directed to solving the problem in the industry of having to use more expensive insulating materials in semiconductors with high-performance yet highly corrosive metal, such as copper, because of the reaction of the metal wiring in the presence of traditional oxide insulating compounds such as Silicon Dioxide (SiO<sub>2</sub>). Applicant's invention provides for a device and method for fabricating such a corrosive metal-based semiconductor such that low-cost oxide-based insulating layers can be deposited over the metal interconnects without damage to the metal interconnects by forming a cobalt silicide layer over a cobalt tungsten phosphor layer.

The significant deficiency of *Lopatin* with respect to claims 6, 12, and 13 is that there is simply no teaching or suggestion whatsoever regarding the use of oxide-based insulating layers or fundamentally the formation of a cobalt silicide clad layer to protect the cobalt tungsten phosphor layer and the underlying copper interconnect from oxidation and fluorinated acid treatments. *Lopatin* actually teaches away from using oxides with copper and CoWP semiconductor devices, disclosing alternative materials such as: “polyarylene ether (PAE), fluorinated aromatic ether (FLARE), fluorinated polyimide (FPI), benzocyclobutene (BCB), hydrogen silsequioxane (HSQ), methyl silsequioxane (MSQ), or xerogel and fluorinated glass.” (*Lopatin*, Column 4 lines 40 – 49).

The Examiner recognizes this deficiency and relies on other references for the subject matter of the cobalt silicide cladding layer.

The remaining references however are similarly deficient. Specifically, the *Shacham-Diamond* reference, the Examiner’s primary reference teaches the creation of a Cu/CoWP/Co/Si structure by depositing *the CoWP barrier layer* followed by Cu which is thereafter annealed to form the resulting structure. Contrary to the Examiner’s assertions, neither this reference nor any other reference teaches or suggests that cobalt and silicon layers should be separately formed over a CoWP layer that is located on a copper wiring.

A careful reading of the reference confirms that the only statement related to cobalt and silicon layer is on page 14 wherein the reference states: “The RBS spectrum of the Cu/CoWP/Co/Si structure formed by electroless CoWP barrier / Cu deposition and annealed at 400 C for 60 min. in vacuum . . . . showed no interdiffusion in deposited films. The reference merely indicates that the specified structure containing the referenced layers is so formed.

Neither this portion nor any remaining portion of the reference indicates that separate Co and silicon layers are formed on the CoWP layer and annealed as asserted by the Examiner. This assertion is only an unsupported conclusion of the Examiner as to the formation of the separate layers prior to annealing. This is the only reference cited for the teaching concerning the cobalt silicide cladding layer or any other cladding layer for that matter that is formed over a CoWP layer on a copper wiring. For this reason alone the rejection is improper and should be withdrawn.

Furthermore, Applicant's invention, is directed to a process by which no separate deposition of cobalt or silicon layers is required. Rather, after deposition of the CoWP layer and within the same apparatus, the substrate (including copper and CoWP layer depositions) is heated in an atmosphere of silane gas, thereby forming a layer of CoSi over the CoWP layer without the need for separate deposition of cobalt and silicon layers, and without the need for separate apparatus to anneal the two layers.

Independent claim 5 from which claim 6 depends specifies forming the cobalt silicide on a surface of the cobalt including layer in a single processing step wherein the cobalt silicide is formed by exposing the cobalt including layer in a silane gas system. Claim 12 requires forming the cobalt silicide on a surface of the cobalt including layer by use of a silane gas atmosphere. Fundamentally, the presence of these limitations provide independent grounds for finding that the rejection of claims 6 and 12-13 is improper.

Yet another deficiency of the rejection is that neither *Shacham-Diamand* nor any other reference teaches or suggests the use of oxide-based insulators formed over the cobalt-silicide layer, as specified by Applicants in claims 6, 12 and 13. In fact, the *Shacham-Diamand* authors teach away from such a result, as the sole stated purpose of applying the

cobalt-silicide layer is to reduce the resistance of the CoWP film, stating said decrease in resistance to be approximately  $5 \mu\Omega/\text{cm}$ . At no point do the authors disclose the use of an oxygen-containing layer applied over the cobalt silicide layer. While the Examiner has stated that it was well-known in the art to use oxygen containing layers in metal-interconnect structures, neither the *Wilson* nor the *Pasch* reference cited by the Examiner teaches or suggests using an oxygen containing layer applied over a cobalt tungsten phosphor layer or over a cobalt silicide layer.

The Examiner has also cited *Sherman* to stand for the notion that the use of silane and oxygen in a CVD process to deposit silicon oxide on a semiconductor surface was well known in the art at the time of invention. Applicants agree that such a process was standard in the industry, just as the use of silicon-dioxide and silicon nitride insulators were standard in common-metal semiconductors. However, with the advent of high-performance but highly corrosive interconnect metals such as copper, these common uses have been replaced by other, more expensive compounds because of the sensitive nature of the metals.

The Examiner provides no prior art that teaches or suggests the combination of cobalt silicide and cobalt tungsten phosphor layers, used as barriers in state of the art copper-metal semiconductors, with the subsequent deposition of oxygen containing layers by using an oxygen containing gas. This is because modern devices using highly corrosive metals such as copper and barrier layers such as cobalt tungsten phosphor are likely to be degraded by any exposure to an oxygen-containing atmosphere.

Applicants have solved this problem by utilizing a three-step process after the metal conductive layer is deposited. Applicants first form a cobalt including layer over the metal conductive member, then form a cobalt silicide layer by exposing the cobalt containing layer

to a silane gas, and finally form an oxygen-including layer over the cobalt silicide layer by adding oxygen to the silane gas atmosphere. *Sherman* fails to teach or suggest such an application of its silicon dioxide deposition process.

*Dubin* teaches the use of copper interconnects and oxide-based insulators separated solely by a CoWP layer, and fails to teach or suggest any formation of a cobalt silicide layer, or deposition of an oxygen-containing layer *after* deposition of the metal layer. Such a device has disadvantages in that it lacks the additional protection provided for by the cobalt silicide layer. The single CoWP layer fails to prevent fluorinated acid reduction and fails to prevent oxidation of the CoWP layer and possibly the metal interconnect when the semiconductor is subsequently placed in an oxygen rich atmosphere for formation of an oxide-layer via a CVD process. Further, *Dubin* fails to disclose any method in which to deposit a subsequent oxide layer without oxidizing the CoWP layer and possibly the copper member.

Applicant's invention set forth in claims 6 and 12-13 specifies a method of manufacturing a semiconductor device containing a conductive member comprising the steps of: 1) forming a cobalt including layer over the conductive member, 2) forming a cobalt silicide layer on a surface of the cobalt including layer by use of a silane gas atmosphere, and 3) forming a layer including oxygen directly on the cobalt silicide layer by adding oxygen to the silane gas atmosphere. None of the references cited by the Examiner teach or suggest such a method containing all three steps. Further, the references actually teach away from such a method.

Accordingly, in light of the foregoing the rejection of claims 6, 12, and 13 should therefore be withdrawn.

**D. The Cited References Fail to Teach or Suggest the Claimed Invention as specified in Claims 8-9.**

None of the references cited by the Examiner, alone or in combination, provides the requisite teaching or suggestion for rendering the subject matter of claims 8-9 invalid as being obvious or anticipated. These references include: *Lopatin* (United States Patent No. 6,259,160), *Dubin* (United States Patent No. 5,695,810), *Shacham-Diamond* “High Aspect Ratio Quarter-Micron Electroless Copper Integrated Technology,” and *Wilson* “Handbook of Multilevel Metallization for Integrated Circuits,” *Sherman* “Chemical Vapor Deposition for Microelectronics,” and Pasch et al.

Claims 8-9 specify a method for manufacturing a semiconductor device containing a conductive member comprising the steps of: forming a CoWP layer over a conductive member, forming a cobalt silicide layer over said cobalt including layer and finally forming an silicon dioxide layer over said cobalt silicide layer. Fundamentally, there is simply no teaching whatsoever in the cited art relating to either the cobalt silicide or cladding layer and the silicon dioxide layer formed over the cobalt silicide.

The significant deficiency of *Lopatin* with respect to claims 8-9 is that there is simply no teaching or suggestion whatsoever regarding the use of oxide-based insulating layers or the formation of a cobalt silicide clad layer to protect the cobalt tungsten phosphor layer and the underlying copper interconnect from oxidation and fluorinated acid treatments. *Lopatin* actually teaches away from using oxides with copper and CoWP semiconductor devices by disclosing alternative materials such as: “polyarylene ether (PAE), fluorinated aromatic ether (FLARE), fluorinated polyimide (FPI), benzocyclobutene (BCB), hydrogen silsequioxane (HSQ), methyl silsequioxane (MSQ), or xerogel and fluorinated glass.” (*Lopatin*, Column 4

lines 40 – 49). The Examiner recognizes this deficiency and relies on other references for the subject matter of the cobalt silicide cladding layer.

The remaining references however are similarly deficient. Specifically, the *Shacham-Diamand* reference, the Examiner's primary reference teaches the creation of a Cu/CoWP/Co/Si structure by depositing *the CoWP barrier layer* followed by Cu which is thereafter annealed to form the resulting structure. Contrary to the Examiner's assertions, neither this reference nor any other reference teaches or suggests that cobalt and silicon layers should be separately formed over a CoWP layer that is located on a copper wiring.

A careful reading of the reference confirms that the only statement related to cobalt and silicon layer is on page 14 wherein the reference states: "The RBS spectrum of the Cu/CoWP/Co/Si structure formed by electroless CoWP barrier / Cu deposition and annealed at 400 C for 60 min. in vacuum . . . . showed no interdiffusion in deposited films. The reference merely indicates that the specified structure containing the referenced layers is so formed. Neither this portion nor any remaining portion of the reference indicates that separate Co and silicon layers are formed on the CoWP layer and annealed as asserted by the Examiner. This assertion is only an unsupported conclusion of the Examiner as to the formation of the separate layers prior to annealing. This is the only reference cited for the teaching concerning the cobalt silicide cladding layer or any other cladding layer for that matter that is formed over a CoWP layer on a copper wiring. For this reason alone the rejection is improper and should be withdrawn.

In addition, the *Shacham-Diamand* reference fails to disclose the use of oxide-based insulators formed over the cobalt-silicide layer, as specified by Applicants in claims 8-9. In fact, the *Shacham-Diamand* authors teach away from such a result, as the sole stated purpose

of applying the cobalt-silicide layer is to reduce the resistance of the CoWP film, stating said decrease in resistance to be approximately  $5 \mu\Omega/\text{cm}$ . At no point do the authors disclose the use of an oxygen-containing layer applied over the cobalt silicide layer. While Examiner has stated that it was well-known in the art to use oxygen containing layers in metal-interconnect structures, neither the *Wilson* nor the *Pasch* reference cited by the Examiner teaches or suggests using an oxygen containing layer applied over a cobalt tungsten phosphor layer or over a cobalt silicide layer formed thereon.

*Dubin* teaches the use of copper interconnects and oxide-based insulators separated solely by a CoWP layer. However, such a device has disadvantages in that it lacks the additional protection provided by the cobalt silicide layer. The single CoWP layer fails to prevent fluorinated acid reduction and fails to prevent oxidation when a semiconductor is placed in an oxygen rich atmosphere for formation of an oxide-layer via a CVD process. This is especially true when attempting to further deposit silicon dioxide via exposure to an oxygen containing chemical vapor epitaxy atmosphere, which will oxidize the protective CoWP film and potentially the copper it is protecting.

Applicant's invention as specified in claim 8 requires a semiconductor device containing 1) a conductive member; 2) a CoWP layer formed over said conductive member; 3) a cobalt silicide formed over said CoWP layer, and 4) a silicon dioxide layer formed over the cobalt silicide. None of the references cited by the Examiner teach or suggest such a structure containing all four semiconductor layers. Further, most of the references actually *teach away* from the specified structure. While one may be motivated to, in hind sight, find such a combination to be obvious in light of its currently disclosed benefits, such a basis for rejection has been held to be inapplicable by the US Court of Appeals for the Federal Circuit.



The Federal Circuit has held that "Combining prior art references without evidence of such a suggestion, teaching, or motivation simply takes the inventor's disclosure as a blueprint for piecing together the prior art to defeat patentability." *In re Dembiczak*, 50 U.S.P.Q.2d 1614, 1617. (C.A.F.C. 1999). Further, "the best defense against the subtle but powerful attraction of a hindsight-based obviousness analysis is rigorous application of the requirement for a showing of the teaching or motivation to combine prior art references." *In re Gartside*, 53 U.S.P.Q.2d 1769 (C.A.F.C. 2000), citing, *In re Dembiczak*, 50 USPQ2d at 1617.

Accordingly, in light of the foregoing the rejection of claims 8-9 is improper and should therefore be withdrawn.

**Conclusion**

In light of the foregoing, Applicant submits that the rejections of all claims are improper for the reasons noted and the rejections should all therefore be withdrawn.

Respectfully submitted,

Date: October 22, 2004

  
Robert J. Depke  
**HOLLAND & KNIGHT LLC**  
131 S. Dearborn, 30<sup>th</sup> Floor  
Chicago, Illinois 60603  
Tel: (312) 263-3600  
**Attorney for Applicant**

(Reg. #37,607)

**CLAIMS ON APPEAL:**

1. (Currently Amended) A semiconductor device comprising:  
  
a conductive member;  
  
a cobalt including layer having oxidation resistive and fluorinated acid resistive properties formed over said conductive member;  
  
a clad layer formed over the cobalt including layer for cladding said cobalt including layer; and  
  
a layer including oxygen formed over the clad layer.
2. (Previously Amended) The semiconductor device as cited in Claim 1, wherein said cobalt including layer is comprised of a cobalt tungsten phosphor layer.
3. (Previously Amended) The semiconductor device as cited in Claim 1, wherein said clad layer is comprised of a cobalt silicide layer.
4. (Previously Amended) The semiconductor device as cited in Claim 1, wherein said cobalt including layer is formed on a copper wiring.
5. (Previously Amended) A method for manufacturing a semiconductor device comprising the steps of:  
  
forming a cobalt including layer on a conductive member;

forming a cobalt silicide layer on a surface of the cobalt including layer in a single processing step wherein said cobalt silicide layer is formed by exposing said cobalt including layer in a silane system gas such that the source of the cobalt is the cobalt including layer and the source of the silicon is the silane gas.

6. (Original) The method of claim 5, further comprising forming a silicon oxide layer on the cobalt silicide by adding oxygen to the silane gas atmosphere.

7. (Original) The method as cited in claim 5, wherein said cobalt including layer is a cobalt tungsten phosphor layer.

8. (Previously Amended) A semiconductor device comprising:  
a conductive member;  
a layer of CoWP formed over the conductive member;  
a layer of cobalt silicide formed over the layer of CoWP; and  
a silicon dioxide layer formed directly on the cobalt silicide.

9. (Previously Added) The semiconductor device of claim 8, wherein the conductive member is a copper wiring.

10. (Previously Canceled)

11. (Previously Added) The method of claim 5, wherein the conductor is a copper wiring.

12. (Previously Amended) A method for manufacturing a semiconductor device comprising the steps of:

forming a cobalt including layer on a conductive member;

forming a cobalt silicide layer on a surface of the cobalt including layer by use of a silane gas atmosphere; and

forming a layer including oxygen directly on the cobalt silicide layer by adding oxygen to the silane gas atmosphere.

13. (Previously Amended) The semiconductor device of claim 12, wherein the layer including oxygen is an oxide layer.


Appl. No. 09/915,145  
Appeal Brief



**CERTIFICATE OF MAILING**

I hereby certify that this correspondence is being deposited with the United States  
Postal Service as First Class Mail on October 22, 2004 in an envelope addressed to:

**Mail Stop Appeal Brief-Patents  
Commissioner For Patents  
P.O. Box 1450  
Arlington, Virginia 22313-1450**

  
\_\_\_\_\_  
Attorney for Applicants